TITLE OF INVENTION:

METHOD FOR TEMPORARILY ISOLATING A DIE FROM A COMMON CONDUCTOR TO FACILITATE WAFER LEVEL TESTING

This is a divisional application based upon U.S. patent application number 09/941,761, filed on August 30, 2001, which is hereby incorporated in its entirety by reference.

FIELD OF THE INVENTION

[0001] This invention relates generally to the fabrication and testing of semiconductor wafers having discrete semiconductor dies. More specifically, the present invention relates to methods of temporarily isolating semiconductor dies from a common conductor during wafer level testing.

BACKGROUND OF THE INVENTION

[0002] In semiconductor manufacture, a large number of often complex electrical devices, also known as dies or integrated circuit (IC) chips, are fabricated on a semiconductor wafer. After fabrication, the dies are subjected to a series of test procedures prior to wafer dicing and packaging to assess the electrical characteristics of the circuitry of each. Dies which are determined to meet specifications are allowed to

continue in the manufacturing process. Those which do not meet specifications are removed from the manufacturing process.

[0003] One series of testing is known as a "wafer level test," which applies stress conditions to the dies on the wafer in an effort to accelerate certain types of failures. Wafer level testing may involve elevated voltage, elevated temperature, elevated humidity or any other condition which a manufacturer deems appropriate to expose failures which can be detected using test equipment.

[0004] To facilitate wafer level testing, a common conductor, e.g., a buss, may be provided which interfaces a plurality of dies under test such that a signal is propagated to the plurality of dies simultaneously. One exemplary common conductor may, for example, connect individual die power inputs to a common power source, e.g., Vcc, Vss. Other common conductors may be used to supply other signals in common to the dies under test.

[0005] The use of a common conductor to supply a signal to multiple dies has its drawbacks. When a die is found to be defective, the defective die must be isolated from the common conductor(s) so that non-defective dies are not affected by electrical conditions occurring at the defective die.

[0006] One way to facilitate high reliability die isolation from a common conductor is by use of a permanent isolation device, for example a fuse. A fuse may be interposed between the common conductor and each die ensuring permanent isolation from the common conductor when the fuse is blown. While fuses and similar permanent isolation devices provide permanent isolation of a device from a common conductor, they do not permit a temporary isolation of a die from a common conductor. Thus individual die isolation and testing cannot be performed without permanently disconnecting a die from the common conductor.

SUMMARY OF THE INVENTION

[0007] The present invention provides a method which facilitates temporary isolation of a die from one or more common conductors during wafer level testing. The one or more common conductors extend over a wafer and are connected to a plurality of dies on the wafers which are undergoing testing. A temporary isolation device (e.g., a diode, transistor or other element) is interposed between each die and the common conductor. The temporary isolation device can be used to isolate a die from the common conductor during wafer level testing whenever such isolation is needed.

[0008] A permanent isolation device may also be provided in the path between each die under test and the common conductor to provide permanent isolation whenever permanent isolation is needed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] These and other aspects and features of the invention will be better understood from the following detailed description which is provided with the accompanying drawings.

[0010] Figure 1 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with an exemplary embodiment of the invention;

[0011] Figure 2 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with a modified embodiment of the invention;

[0012] Figure 3 shows a simplified process sequence for isolating and testing dies using the Fig. 1 or Fig. 2 embodiment of the invention;

[0013] Figure 4 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with another modified embodiment of the invention;

[0014] Figure 5 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with another modified embodiment of the invention;

[0015] Figure 6 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with another modified embodiment of the invention;

[0016] Figure 7 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with another modified embodiment of the invention;

[0017] Figure 8 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with another modified embodiment of the invention; and

[0018] Figure 9 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with another modified embodiment of the invention.

[0019] Figure 10 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with another modified embodiment of the invention.

[0020] Figure 11 shows a simplified schematic diagram of a portion of a semiconductor wafer constructed in accordance with another modified embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0021] The invention provides the capability to perform wafer level testing while temporarily isolating a die for testing from other dies which are otherwise in electrical communication with a common conductor. In the invention, at least one temporary isolation device is provided between each die and a common conductor to temporarily electrically isolate the die from the common conductor. The temporary isolation device may be a diode, transistor or other element. When a diode is used it can be reverse biased such that the individual die is isolated from the common conductor. The invention also provides a temporary isolation testing system and procedure which is compatible with conventional test equipment already in use.

[0022] Temporary isolation of each unsingulated die on the wafer from the common buss can be performed with the invention, such that it may be determined if an individual die meets the required specifications that allow the die to continue in the manufacturing process. If a die is deemed to not meet the required specifications during this temporary isolation, it may be subjected to repair or permanent isolation from the common conductor.

[0023] To simplify discussion, a fuse will be described as one exemplary form of a permanent isolation device which can be employed in the invention, and a diode will be described as one exemplary form of a temporary isolation device.

However, it must be understood that any one of a variety of devices may be used as a permanent and temporary isolation devices and thus the invention is not limited to fuses or diodes to accomplish the permanent and/or temporary isolation functions. Non-limiting examples of other permanent isolation devices include several electrical connections or other electrical circuits or devices which permanently isolate a die from a common conductor. Non-limiting examples of other temporary isolation devices include transistors, or other electrical circuits or devices which can temporarily isolate a die from a common conductor.

[0024] Also, for simplicity, a common conductor will be discussed below as one or more power supply conductors; however, the common conductor can be used to supply any signal to plural dies connected to it.

[0025] The invention will now be explained with reference to Figs. 1-10. Fig. 1 discloses one exemplary embodiment of the invention. A portion of a wafer is shown as containing a plurality of dies 5 which are to be tested before die singulation. A common conductor 1 is provided on the wafer and is used to supply a first signal, for example, a positive Vcc voltage, to the individual dies. Likewise, a common conductor 3 is provided on the wafer and is used to supply a second signal, for example, a Vss voltage (ground), to the individual dies.

[0026] The common conductors 1 and 3 may supply any signals necessary for die operation or testing and thus, as noted, are not limited to supplying first and second voltage signals, e.g. Vcc and Vss. The common conductor may be a single conductor or may be part of a group of common conductors which provide signals to the dies 5.

[0027] A plurality of probe pads 9 are provided in direct electrical communication with the common conductor 1, each in proximity to a die 5 on the wafer. A probe pad 11 is provided on each die 5 on the wafer in proximity to a probe pad 9 on the wafer. A permanent isolation device 7 (e.g. fuse) may be interposed between the common buss 1 and a probe pad 11. A probe pad 17 is provided on each die 5 and is connected to, for example, the normal Vcc voltage input terminal of the die. A temporary isolation device 19, e.g., diode, is provided on each die 5 between each probe pad 17 and probe pad 11. The diode 19 is installed such that it is operative in a forward bias manner during wafer level testing allowing a signal to pass from common conductor 1 to probe pad 11 and to probe pad 17. When temporary isolation is needed, the diode is reverse biased thereby isolating the die from the common conductor 1.

[0028] A plurality of probe pads 13 are provided in direct electrical communication to another common conductor 3 each in proximity to a die 5 on the wafer. A probe pad 15 resides on each die 5 in proximity to the closest probe pad 13 on

the wafer. A permanent isolation device 7 (e.g. fuse) may be interposed between each probe pad 13 and a probe pad 15. A probe pad 21 is provided on each die 5 and is connected to, for example, the normal Vss voltage input terminal of the die. A temporary isolation device 19 (e.g. diode) is installed on the die 5 between each probe pad 21 and probe pad 15. The diode 19 is installed such that it is operative in a forward bias manner during wafer level testing allowing a signal to pass between probe pad 21 and probe pad 15. When temporary isolation is needed, the diode 19 is reverse biased thereby isolating the die 5 from the common conductor 3. It should be recognized that while Fig. 1 shows a permanent isolation device 7 (e.g. fuse) and a temporary isolation device 19 (e.g. diode) interposed between each common conductor and the die, it may be desirable to also have some common conductors which are connected directly to the dies 5 without interposed permanent or temporary isolation devices. Also, although Fig. 1 shows the permanent isolation devices 7 fabricated on the wafer off the dies 5 and the temporary isolation devices 19 fabricated on the dies, it is possible to fabricate both off the dies 5 or both on the dies 5, or with the temporary isolation device 19 off the dies 5 and the permanent isolation device 7 on the dies. It is also possible to provide the common conductor on an external interface, e.g. a test head or a probe card, and provide one or both of the permanent isolation device 7 and temporary isolation device 19 on the external interface.

[0029] As can be seen in Fig. 1, when the diodes 19 between pads 11 and 17 and pads 21 and 15 are reverse biased during probe testing procedures of an individual die, only a small amount of leakage will be observed passing to the common wafer conductors 1 and 3 through the permanent isolation device, e.g. fuse 7. Accordingly, each die may be individually tested with a first and second signal, e.g. Vcc and Vss respectively provided through probe pads 17 and 21, without affecting other dies connected to the common conductors 1 and 3. If during such individual testing a die is found to be defective, the permanent isolation device 7 associated with the defective die may be used by means well known in the art (e.g. fuse blowing) to permanently isolate the die from the common conductors 1 and 3 thereby enabling the common conductors to effectively power the serviceable dies during wafer level testing procedures.

[0030] Fig. 1 shows the permanent isolation device 7, e.g., fuse, provided on a wafer and off the dies 5 and between pads 9 and 11 and between pads 13 and 15. However, as noted, the permanent isolation device can be provided at other locations, including on each die 5, or on an external interface, between a common conductor 1 and a die signal pad on the die requiring a signal from the common conductor. Moreover, the temporary isolation devices 19, e.g., diodes, may be directly connected to a respective common conductor, e.g. 1, 3 with the permanent isolation devices being connected between the temporary isolation devices and die.

[0031] For example, Fig 2 shows one alternative embodiment of the invention where the temporary isolation device 19, e.g. diode, between pads 15 and 21 is omitted. Fig. 2 also shows omission of the permanent isolation devices 7, e.g. fuse, between pads 9 and 11 and 13 and 15. Other modified embodiments are described below with reference to Figs. 4-11.

[0032] Fig. 3 shows a simplified processing sequence used for testing each die 5 in Fig. 1. First, in processing segment 101, single die level signals are applied from an external interface to the pads 17 and 11 and 21 and 15 to supply signals to the temporary isolation device(s). Other probes of the external interface may be applied to other signal pads of each die 5 during testing. This reverse biases the diodes used as temporary isolation devices 19, thereby isolating a die 5 from the common conductors 1 and 3. In processing segment 103, testing of an isolated die 5 is performed. If the testing reveals that a die 5 should be permanently isolated, then in processing segment 105, the permanent isolation devices 7 are activated, e.g., fuses blown, to permanently isolate defective dies 5 from the common conductors 1, 3. As shown in processing sequence 107, when the wafer is subjected to wafer level testing conditions, including, for example, wafer level burn-in, signals are applied to conductors 1, 3 which during operation forward bias the diodes 19, permitting common conductors to supply desired signals to all dies still connected to the common conductors. Tests are then conducted

with all dies 5 receiving common signals from the common conductors.

[0033] The processing sequence of Fig. 3 may be varied from that shown to perform testing or other operations which require temporary isolation of dies 5 from one or more common conductors. For example, die isolation and individual die testing using the Fig. 1 embodiment, may be accomplished after signals are commonly applied to all dies through the common conductors 1 and 3 (segment 107). The permanent isolation devices 7, e.g. fuses, can be opened, e.g. fuses blown, either automatically or manually when defective dies are identified when signals are applied to conductors 1, 3. The permanent isolation devices may also be opened when signals are applied directly to the die pads 17 and 21 and defective device dies 5 are found. Permanent isolation devices 7, such as fuses, may be activated by use of any technology which is appropriate for providing permanent isolation of dies from a common conductor. When fuses are used, the fuse itself can be automatically blown when excessive current passes through it, or it can be opened by laser, mechanical severance, applying a sufficient high voltage across it, or other technique.

[0034] Figs. 4 through 11 illustrate other alternative embodiments of the invention. Fig. 4 illustrates an embodiment where the permanent isolation device 7, e.g. a fuse, and a temporary isolation device 19, e.g., a diode, are provided on a wafer

between a common conductor 31 and a die 5. Probe pads 33, 35 and 37 are also shown. In this embodiment, both the permanent 7 and temporary 19 isolation devices are provided off die, for example, in the street area of a wafer.

[0035] Fig. 5 illustrates an embodiment where the permanent isolation device 7, e.g. fuse, and temporary isolation device 19, e.g. diode, are provided on a die 5, and a pair of spaced probe pads 45a, 45b are used which can be bridged by a conductor on an external interface to connect die 5 to common conductor 31. Pad 45b is provided on the die while pad 45a is provided off the die 5.

[0036] Fig. 6 illustrates an embodiment of the invention in which the permanent isolation device 7, e.g. a fuse, is provided off the die, the temporary isolation device 19, e.g. a diode, is provided on the die and spaced pads 45a, 45b which can be bridged by a conductor on an external interface and which are used to connect die 5 to the common conductor 31.

[0037] Fig. 7 illustrates an embodiment of the invention in which both the permanent isolation device 7, e.g. fuse, and the temporary isolation device 19, e.g. diode, are provided off the die 5 and a pair of spaced pads 45a, 45b which can be bridged with a conductor on an external interface which are used to connect die 5 to the common conductor 31. Here pad 45a is provided off die 5, while pad 45b is provided on the die 5.

[0038] Fig. 8 illustrates an embodiment of the invention similar to Fig. 4, but where the locations of the permanent and temporary isolation devices 7, 19 are reversed.

[0039] Figs. 9 and 10 illustrate embodiments similar to Fig. 4, but were the temporary isolation device 19' is shown as a transistor connected as a diode. Figs. 9 and 10 differ in the type of transistor and associated connections which make it function as a diode.

[0040] Fig. 11 illustrates an embodiment similar to Fig. 4, but where the temporary isolation device 19'' is a controlled transistor with the control signal being supplied via a probe pad 43. The applied control signal may originate at an external interface.

[0041] While the invention has been described and illustrated with respect to one or more common conductors, e.g. 1, 3, 31, which are provided on a wafer, the common conductors can instead be provided on an external interface used during wafer level testing.

[0042] Also, during temporary isolation, individual dies 5 may be tested in a predefined order or simultaneously.

[0043] While exemplary embodiments of the invention have been described and illustrated, it should be evident that many alterations, modifications and variations can be made without departing from the spirit or scope of the invention. Accordingly, the invention is not to be considered as limited by the descriptions and illustrations provided, but is only limited by the scope of the appended claims.